Theoretical Aspects of Fault Isolation on High-Power DC Lines Using Resonant DC/DC Converters

Dr Dragan Jovcic,
School of Engineering,
University of Aberdeen,
Aberdeen, AB24 3UE, UK
Tel 01224 272 336
Email: d.jovcic@abdn.ac.uk

and
Professor Boon Teck Ooi,
Electrical Engineering,
McGill University,
Montreal, H3A 2A7,
Canada,
Email: boon-teck.ooi@mcgill.ca.

Abstract*—This paper investigates DC fault current limiting and interrupting capability of a multi MW resonant DC/DC converter which is proposed for applications with High Voltage Direct Current (HVDC) systems. The converter can be used as a DC circuit breaker or as a multifunctional unit: DC transformer, regulating element and DC circuit breaker. The study is primarily concerned with the inherent converter responses, in the first several milliseconds after the fault, and prior to any controller action. A detailed converter design is given to prevent fault propagation through the converter even for most severe faults on low voltage or high voltage terminals. The analytical modelling proves that the converter will internally reduce power transfer during fault conditions. The simulation on PSCAD/EMTDC shows that converter operates uninterrupted through most severe faults, the switch turn-off time is not violated and inherent stabilising properties prevent any overvoltage or extreme currents. The converter can respond like high-impedance circuit on the unfaulted terminals. The impact of unbalanced DC line faults on a bipolar DC system is also discussed. The detailed PSCAD tests with a 200MW DC/DC converter interconnecting ±44kV and ±250kV DC lines demonstrate the ability to prevent fault propagation even for most severe DC line faults. The interaction with other HVDC converters in case of faults is also demonstrated.

***Index Terms*— DC-DC power conversion, thyristor converters, High Voltage DC transmission.**

I. Introduction

All the HVDC installations worldwide operate as two terminal systems, but there has been significant incentive for development of multiterminal HVDC and HVDC tapping [1]. The latest HVDC based on VSC converters [2] has been applied in a dozen projects and it is being studied for development of high-power DC grids for subsea systems in oil and renewable industries. In recent years we have seen an increasing number and rating of DC power sources, like fuel cells, photovoltaics, wind farms and energy storage elements that would ideally be connected to DC collecting grids at medium and high voltage [3,4,5]. The proposed European North Sea Supergrid and DESERTEC concept will be based on high-power DC networks.

The development of multiterminal HVDC and DC networks will require significant further advances in the two key high-power components: DC Circuit Breaker (CB) and DC transformer. A DC circuit breaker enables isolation of a faulted line or a unit. A DC transformer can transform DC voltage levels to maintain optimum costs and losses.

The fault protection is much more challenging with DC than AC networks for the following reasons: 1) there are no zero crossings of DC fault current, 2) the series impedance (with VSC based converters) is very small leading to very steep rise of fault current, 3) interrupting large DC current causes severe overvoltages and 4) the equipment is usually more sensitive to overvoltages and overcurrents. There are no operational CBs on HVDC systems worldwide, except for one very low power ground-return installation in Japan [6].

The researched technologies for DC CB [4-8] can be grouped in mechanical and solid state solutions. The mechanical DC circuit breakers [6] consist of a conventional AC circuit breaker supplemented with a parallel resonant circuit. This solution demands high overrating, but most importantly, it has long operating times (*20-100ms*) and therefore it will not be suitable with VSC based HVDC. In such long interval, the fault current on VSC systems will reach extremely high values which will be beyond interrupting capability of circuit breakers. The hybrid topologies combine a mechanical switch with electronics-driven resonant circuit but the operating times are still too long for VSC protection [7].

A future DC network based on VSC will need some solid-state DC CB. A single electronic switch (a GTO/IGBT) may be strategically located at DC line ends and supplemented with fast mechanical switches [4]. Alternatively the anti-parallel diodes are replaced with symmetrical GTOs [5]. These solutions will have fast DC fault-isolation capability but they will have high costs and losses. Assuming that GTO control reaction time is below *5ms*, because of low series impedance with VSC HVDC systems the current will still rise at very high levels (above *10pu*) before it is intercepted. IGBT/GTOs typically have peak interruption capability of only around *200%* of nominal current, and in practice this implies significant overrating in normal operation. Locating such switches at all DC lines would be prohibitively expensive. A further significant issue with fast interruption of DC fault current is the resulting overvoltage [7]. The DC fault current must be interrupted in short interval while

the current magnitude is within the switch turn-off capability. The overvoltages are proportional to current derivative and very high energy surge arresters are needed with all solid-state circuit breakers [5,7]. In cases of long DC lines, the energy capability of conventional surge arresters may not be adequate and supplementary energy dumps may be required.

With traction drives, the DC circuit breaker is commonly based on thyristors which can take larger fault currents [8]. However the complexity, costs and overrating are high.

Some DC/DC converters will have capability to limit the magnitude of fault current (because of internal inductors) but in most cases significant switch overrating is required to cope with fault conditions [5,9]. The aerospace industry studied some potentially useful properties of series resonant topologies under fault conditions in the early *1980's* [10], but other drawbacks have prevented industry applications.

Recently, a new high-power step up/down DC/DC converter based on resonant circuits has been proposed, and it has been studied with a *5MW, 4kV/80kV* application [11]. The converter is capable of achieving very high stepping ratios at high powers, without use of iron core transformers.

This paper takes the resonant topologies [11] and studies design options to provide isolation of DC faults. The aim is to provide controllable converter operation under external DC faults and to limit the internal variables close to rated levels. If there is no significant overcurrent or overvoltage under faults, the speed of converter control action becomes less important. Assuming that the converter continues normal operation during faults it can be controlled to gradually reduce current over loner time period, and eventually to become blocked to permanently isolate the fault.

II. CONVERTER TOPOLOGY AND FAULT STUDIES

A. High Power Bidirectional DC transformer

Figure 1 shows the bidirectional version of the high power DC transformer [11]. It consists of two resonant *LC* circuits, back to back connected and sharing a common capacitor. This topology uses bidirectional switches and achieves fast power reversal by reversing currents in both circuits (I_1 and I_2). A unidirectional version would have half the switches, and slow power reversal may be possible with mechanical contactors.

In step up mode, the T_1 and T_2 thyristor pairs are sequentially fired at *50%* duty ratio at f_s switching frequency, as shown in Figure 2. The inductor L_1 creates a resonance with C_r which enables V_c voltage increasing and zero-current turn on and off of T_1-T_2. All the switches should have reverse blocking capability but circuit topology provides current commutation and therefore thyristors are suitable. The high voltage circuit resonance (L_2-C_r) enables zero current switchings of T_5-T_6. In step down mode the operating principle is similar, but T_3-T_4 and T_7-T_8 thyristors are employed instead. The maximum operating frequency f_{smax} is primarily dependent on the minimum turn off time of low voltage switches $T_{off1min}$:

$$f_s < f_{s\max} = 1/(4T_{off\,1\min}) \tag{1}$$

Once f_s is known, the principal converter design equation is:

$$I_2(V_2 - V_1)/(V_1V_2) = 2C_r f_s, \tag{2}$$

where manipulation in the switching frequency f_s, enables linear control. From (2) we conclude that the converter power transfer is determined by C_r and f_s. Assuming operation at the border of discontinuous mode, the inductor L_1 is determined:

$$L_1 \le 1/\left(\pi^2 f_s^2 C_r\right) \tag{3}$$

The high voltage switches are synchronized to operate at the same frequency f_s, but there is freedom in choosing firing angle for T_5-T_8 (α_{2u} for step up and α_{2d} for step down). The high voltage circuit inductors (L_{2u} for step up and L_{2d} for step down) are smaller than L_1 and less critical for the operation. The inductor for step down mode, L_{2d} and the firing angle α_{2d} can be determined using the design study in [11]. The design of step-up inductor L_{2u} is influenced by the high-voltage faults, as described in section IV.

A PI feedback controller typically manipulates f_s to regulate DC current (either I_1 or I_2) in a feedback manner.

B. Tests system

The test system is a high-power *200MW* DC/DC converter interconnecting *±44kV* and *±250kV* DC (stepping ratio *n=5.7*). Such converter may be utilized in connecting a low voltage DC feeder to existing *±250kV* HVDC lines, as required in future DC networks. A detailed test system model is developed on PSCAD platform and all parameters are in the Appendix.

C. Fault studies

We investigate the worst case zero-impedance faults at converter terminals V_1 and V_2 (V_1<V_2). There are four possible fault scenarios:

A. Fault on V_1 for step-up operation (V_1 to V_2 transfer).

B. Fault on V_2 for step-up operation (V_1 to V_2 transfer).

C. Fault on V_1 for step-down operation (V_2 to V_1 transfer)

D. Fault on V_2 for step-down operation (V_2 to V_1 transfer).

Considering that the converter uses reverse blocking switches, the faults *A.* and *D.* are trivial since they are occurring "upstream" of the converter, and they will only interrupt power transfer through the converter. The faults *B.* and *C.* are known to disturb operation of typical converters and they will be further studied in detail.

If there is a fault at one of the terminals, the time-domain converter response will be undergoing four sequential stages:

- **Stage 1.** The initial transient lasting in the order of few *ms*, (1-2 cycles at around *500Hz* switching frequency). The internal converter variables experience peak fault values, and controller is inactive.
- **Stage 2.** After several cycles, a new steady-state operation under fault conditions is established (if exists). The stages 1 and 2 define the converter's natural response to faults since the controller will be inactive in this period.
- **Stage 3.** Considering all delays in the transducers, processing and firing circuits, it is conservatively assumed that a normal controller response time will be around *10-30ms*. After this delay, the controller can reduce operating frequency or interrupt firing pulses in line with fault management strategy [5].
- **Stage 4.** In case that the fault is permanent the converter will reduce the operating frequency to *0* in stage 3, and converter is blocked. In stage 4, the off-load mechanical switches open and the fault isolation is complete.

The fault controller design is a known concept [5] and therefore stages 3 and 4 are not considered in this research. The design is primarily concerned with stages 1 and 2 assuming that the controller is inactive, i.e. operating frequency f_s is constant.

III. CONVERTER DESIGN FOR V_1 FAULTS (FAULT C)

In order to provide controllable operation under fault conditions, two principal conditions should be met:

1. The circuit-allowed switch turn-off time (T_{off1} for low voltage circuit, and T_{off2} for high voltage thyristors) should be larger than the minimum turn off time for the particular switches. For the employed Silicon Power thyristors $T_{offmin}=400\mu s$. If this condition is violated, there will be unwanted thyristor turn on, V_c will collapse, and fault will propagate through the converter.

2. The magnitude of all converter variables should be within the rated limits for the electronic components. It is crucial to monitor peak switch currents (I_{1pk} and I_{2pk}) and peak capacitor voltage (V_{cpk}).

Figure 3 shows the PSCAD simulation of first two cycles after a most severe fault on low voltage side (V_1*:88kV->0kV*). For comparison, the capacitor voltage is shown for the case of fault (V_c) and in the case of no fault (V_c^{nf}). The low voltage circuit conducts in A-D and the high voltage circuit conducts in B-C interval, however depending on the circuit conditions point C can occur before or after point D.

The equations for capacitor voltage V_c and current I_1 in interval A-B ($t_A<t<t_B$) can be derived using the circuit analysis rules as described in [9,11]:

$$V_c = -V_1 - (-V_{cA} - V_1)\cos(\omega_1 t) \tag{4}$$

$$I_1 = (-V_1 - V_{cA}) / Z_1 \sin(\omega_1 t) \tag{5}$$

where V_{cA} is the initial value of V_c at the instant of rotation. As the first approximation, it can be assumed as V_{cA}=-V_2. The low voltage circuit constants are $Z_1 = \sqrt{4L_1 / C_r}$, $\omega_1 = \sqrt{1/(L_1 C_1)}$.

In the B-D interval (t_B<t<t_D) both high voltage and low voltage circuits will be conducting implying that there are three dynamic equations. They can be solved in time domain as discussed in [11]:

$$V_c = \frac{L_1 V_2 - L_2 V_1}{L_1 + L_2} + \left(V_{cB} + \frac{L_2 V_1 - L_1 V_2}{L_1 + L_2} \right) \cos(\omega_e t) + \frac{L_1 I_{1B}}{L_1 + L_2} Z_e \sin(\omega_e t) \tag{6}$$

$$I_1 = -\frac{V_1 + V_2}{L_1 + L_2} t - \left(\frac{L_2 V_1 - L_1 V_2}{L_1 + L_2} - V_{cB} \right) \frac{L_2}{L_1 Z_e} \sin(\omega_e t) + I_{1B} \left(\frac{L_1 + L_2 \cos(\omega_e t)}{L_1 + L_2} \right) \tag{7}$$

$$I_2 = \frac{V_2 + V_1}{L_1 + L_2} t + \left(\frac{V_2 L_1 - V_1 L_2}{L_1 + L_2} - V_{cB} \right) \frac{\sin(\omega_e t)}{Z_e} + I_{1B} L_1 \frac{\cos(\omega_e t) - 1}{L_1 + L_2} \tag{8}$$

where $Z_e = \sqrt{4L_{2d}(L_1 + L_{2d})/(L_1 C_r)}$, $\omega_e = \sqrt{(L_1 + L_{2d})/(L_1 L_{2d} C_r)}$, and it is assumed that a local time axis starts at point B (t_B<t<t_D). If point C falls after D, the equations in D-C interval, are:

$$V_c = V_2 - (V_2 - V_{cD})\cos(\omega_2 t) + Z_2 I_{2D} \sin(\omega_2 t) \tag{9}$$

$$I_2 = I_{2D} \cos(\omega_2 t) + (V_2 - V_{cD}) / Z_2 \sin(\omega_2 t) \tag{10}$$

assuming $Z_2 = \sqrt{4L_{2d} / C_r}$, $\omega_2 = \sqrt{1/(L_{2d} C_1)}$ and a local time axis (t_D<t<t_C).

The V_c zero-crossing and the peak current I_{1pk} will typically occur at around 90^o, which falls in A-B interval, since high voltage thyristors are fired typically around $\alpha_{2d}=120^o$. Therefore, the turn off time T_{off1}, which is defined by the next V_c zero-crossing (point H) can be calculated using (4):

$$T_{off1} = \left(\cos^{-1}(V_1/(V_2 - V_1))\right)/\omega_1 \qquad (t_A<t<t_B) \tag{11}$$

If V_1 reduces, it is evident from (11) that the turn off time reduces, however this reduction is very small. In the practical system in Figure 3, point *H* marginally moves to the left. Figure 4 shows the percentage reduction in turn off time $\Delta T_{off1}/T_{off1}$ as the function of stepping ratio $n=V_2/V_1$ ($3<n<20$), for a zero-impedance fault on V_1. It is seen that in the worst case (low stepping ratio) the reduction in T_{off1} is only *15%*. Normally a much larger margin will be incorporated when selecting operating frequency in (1).

Using (5) we deduce that peak current I_{1pk} will be larger than in no-fault case I_{1pk}^{nf}:

$$I_{1pk} = V_2\sqrt{C_r/(4L_1)} > I_{1pk}^{nf} = (V_2 - V_1)\sqrt{C_r/(4L_1)} \qquad (t_A<t<t_B) \tag{12}$$

The largest fault current increase, i.e. if stepping ratio is $n=3$, is calculated to be around *50%*, as seen in Figure 4. The test system has $n=5.7$, and the increase is around *20%* which is consistent with PSCAD results in Figure 3. We can conclude that the switches will readily tolerate the above fault current level during stages 1 and 2.

Using (4) we derive that in A-B interval the capacitor voltage V_c is always higher than in no-fault case V_c^{nf}:

$$0 < V_c - V_c^{nf} < 2V_1 \qquad (t_A<t<t_B) \tag{13}$$

Using (13) we also concluded that V_c under fault conditions leads the unfaulted voltage curve (although by a small amount). As a consequence it is clear that $V_{cB}>V_{cB}^{nf}$, and this will have crucial impact in reducing I_2.

Using (4) and (5) we determine the variables at the instant of firing high voltage thyristors in point B: $V_{cB}=V_c(\alpha_{2d})$, $I_{1B}=I_1(\alpha_{2d})$, which is then replaced in (6)-(8) to calculate I_2. It can be readily shown that I_2 will be lower as V_1 reduces. The above conclusion can be simply analytically confirmed by expressing the I_2 derivative with respect to voltage V_1 using (8):

$$\frac{dI_2}{dV_1}(L_1 + L_{2d}) = t + (1 - L_2 - \cos\alpha_{2d})\frac{\sin(\omega_e t)}{Z_e} - \sin\alpha_{2d}\,\frac{L_1(\cos(\omega_e t) - 1)}{Z_1} \qquad (t_B<t<t_D) \tag{14}$$

The above derivative is always positive, and therefore current I_2 will be reducing as the voltage V_1 reduces. Alternatively, the same conclusion can be derived graphically from Figure 3, considering the surface area between V_{cr2} and V_2.in B-C interval. The energy balance on inductor L_{2d} implies that this area is always symmetrical around V_2 and therefore $V_{cB}>V_{cB}^{nf}$ implies that I_2 is smaller under faults. If the converter dynamics are neglected, we can employ the basic steady-state equation (2), and assuming high stepping ratio is high ($(V_2-V_1)/V_2\approx 1$), it is similarly confirmed that current I_2 reduces as V_1 reduces. This inherent stabilising feedback loop is highly important property of this converter family, since it restricts power flow into the converter during faults.

In order to study capacitor peak voltage V_{cpk} under faults we need to solve (4), (6) and (9) in iterative manner to determine a balanced operating point. However we can simplify study considering the extreme fault condition $V_1=0$, and assuming that $I_2=0$, as concluded above. Consequently, we can use (4) for the whole A-D interval and we deduce that the peak capacitor voltage V_{cpk} will stay unchanged:

$$V_{cpk}=V_{cpk}^{nf}=V_c(\pi)=-V_{cA}. \tag{15}$$

As seen in Figure 3, while V_c marginally increases in *A-B* interval, in *B-C* interval I_2 reduces implying that less energy is transferred to capacitor C_r. and V_c lowers. It is very important property that an internal stabilizing loop prevents overvoltage under fault conditions.

A further consequence of reduced I_2 in B-C interval is that the turn off time in high-voltage circuit (T_{off2}) actually increases after the fault, enabling better commutation margin of high-voltage switches.

The iterative methods are now applied to (4)-(10) (and verified using detailed PSCAD tests) in order to determine the magnitude of the crucial variables under V_1 faults of varying severity. Figure 5a) shows the values for the I_1, V_{cpk} and I_2 as the function of voltage V_1. It is seen that the current I_1 marginally increases and the peak capacitor voltage V_{cpk} remains unchanged. The current on unfaulted side I_2, proportionally reduces as V_1 reduces. The converter becomes open circuit on high-voltage side for extreme faults on low voltage side, although it can be demonstrated current I_2 cannot reduce to *0* even with $V_1=0$. The very small value of I_2 current under $V_1=0$ operation can be absorbed by internal converter losses.

IV. CONVERTER DESIGN FOR V_2 FAULTS (FAULT B)

A. Symmetrical fault

Figure 6 shows the transient response for a high voltage fault (V_2:*500kV -> 0kV*) in step up mode. The capacitor voltage waveform is shown for fault case V_c and no-fault case V_c^{nf}, and it is seen that V_c will not be affected until the next interval B-C when high-voltage thyristors are conducting.

The same equations (4)-(10) describe the circuit except that both currents (I_1 and I_2) have opposite sign. Using (6) it can be shown that the waveform for V_c also leads the unfaulted voltage curve. Consequently, $V_{cA}>V_{cA}^{nf}$, the voltage V_{cA} is closer to V_1 under faults, and this implies that I_1 reduces. Therefore, the same internal stabilizing mechanism operates in fault B, which reduces current on the opposite terminals.

The peak capacitor voltage V_{cpk} also has stabilizing feedback loop that prevents any overvoltage because of reduced power input through I_1.

It can be observed from Figure 6 that the turn off time T_{off1} actually increases under the V_2 fault, except in the first cycle immediately after the fault, where it is significantly reduced. This first post-fault cycle becomes crucial for commutation failure and for converter design.

Under the $V_2=0$ faults, the zero-crossing of voltage V_c will move to B-C interval (when high-voltage switches are conducting) considering that V_c is symmetrical around V_2. Therefore the high voltage circuit parameters (C_r-L_{2u}) will define the turn off time in the low voltage circuit (T_{off1}).

There are two design options to provide sufficient T_{off1}:

1.) Increasing the firing angle for high voltage thyristors (α_{2u}). This simple approach however implies increase in peak capacitor voltage (V_{cpk}) and may also lead to stability issues. Simulation studies indicate that a value of around α_{2u}*=150-160deg* is a good compromise.

2.) Calculating a suitable L_{2u}. To simplify study, we assume that influence of I_1 can be neglected during the fault $V_2=0$, since it has been proven that I_1 will be reducing. Under the assumptions $I_1=0$ and $V_2=0$, the equations for the time interval to V_c zero crossing and the peak current I_{2pk} can be derived using (10):

$$T_{off1} = \sqrt{L_1 C_r}\,(\alpha_{2u} - \pi) + \sqrt{L_{2u} C_r}\,\pi / 2 \tag{16}$$

$$I_{2pk} = V_{cpk}\sqrt{C_r /(4L_{2u})} \tag{17}$$

The first term in (16) is typically small since α_{2u} is close to π. Therefore the allowed turn off time is approximately ¼ of the L_{2u}-C_r resonant cycle. Under these assumptions (16) is similar to (11) and L_{2u} should be comparable size to L_1. In our test system L_1 is selected with a considerable margin in (1) and (3), whereas L_{2u} is chosen to tightly satisfy (16) and therefore L_{2u} is calculated as $L_{2u} \approx 0.5 L_1$.

The equation (17) can be used to estimate the worst case peak fault current I_{2pk}. Considering the chosen $L_{2u}=14mH$, (17) gives peak current around *7.5kA*, on approximately *1ms* half-cycle, which is comparable to the magnitude obtained with PSCAD simulation in Figure 6. Typical thyristors will have peak overcurrent *5-10pu* specified on a *10ms* half-cycle, and therefore the transient level of I_{2pk} can be tolerated by thyristors in a short interval.

As a simple guiding rule, L_{2u} should be comparable to L_1, in order to provide immunity from worst-case V_2 faults. This large value of L_{2u} will not cause negative consequence during normal step up operation except for marginally increased V_{cpk} and reverse recovery losses in T_5-T_6. However, the inductor for step down operation L_{2d} should have much smaller values. The value for L_{2d} is independently calculated considering the turn off time (T_{off2}) and current derivatives (dI_2/dt_{max}) in T_7-T_8 as it is discussed in [11]. For these reasons it is recommend using two separate inductors on high-voltage side, a large one for step up and a smaller inductor for step down mode. In practice, a single large inductor can be built, where the smaller L_{2d} inductance is implemented as a tap on L_{2u}.

Figure 5b) shows the converter steady-state variables for fault B of varying severity (progressively reduced voltage V_2). The behavior mirrors that for fault C in Figure 5a). The current on faulted side (I_2) remains constant and only for extremely low voltages it increases to around *5p.u.* This is a reactive current oscillating in L_{2u}-C_r circuit, which lasts for a short period until controller reacts in stage 3. The peak capacitor voltage (V_{cpk}) reduces and clearly there is no danger of overvoltage.

In some cases it might be beneficial to have a single high voltage inductor L_2. This option will lead to higher peak voltages V_{cpk} and lower operating frequency in step down mode. The Appendix gives all the data for this design option.

B. Unsymmetrical faults

The above studies consider worst-case pole-pole DC faults, but a pole to ground fault may be more common in a practical system. It is assumed that the DC sources V_1 and V_2 are solidly grounded at central points, as it would be common with bi-polar HVDC systems. The rotating capacitor C_r uses high-impedance grounding at the center, as shown in Figure 1.

Figure 7 shows the converter response after a zero impedance fault on positive pole of V_2 (V_{2p}:*250kV->0kV*) All the variable labels have additional subscript for positive (*p*) or negative (*n*) pole. It is seen that the average current on unfaulted side I_1 and power transfer halve and controllable operation is maintained.

The share of the average current during the fault is shown in Table 1. The ground return current on the unfaulted side will be 32% of the pre-fault current. Because of the thyristor overload on the faulted pole and the ground return current, the bipolar

operation should not be allowed, and the positive pole on V_1 terminal should be bypassed. Under this fault management, the whole system can continue to operate at negative poles and transferring half the power.

TABLE 1. CURRENT SHARE AFTER POLE TO GROUND FAULT ON V_{2p}.

Current	I_{1p}	I_{1n}	I_{2p}	I_{2n}
% of pre-fault value	*57%*	*36%*	*267%*	*66%*

V. INTERNAL CONVERTER FAULTS

The internal converter faults can occur because of control system malfunctioning. The worst scenario is the case where two switches in the same branch are simultaneously fired (T_1 and T_2), leading to short circuit on converter terminals. However observing Figure1 it is concluded that such fault would not short the capacitor Cr, and the DC terminals would only be shorted through inductors L_1 or L_2. Therefore power transfer would be interrupted but the current derivative would be constrained and the fault could be interrupted by the next DC/DC converter either on low voltage or high-voltage DC lines.

VI. INTEGRATION STUDIES

A. PSCAD test system with an HVDC tap

A detailed PSCAD model for the DC/DC converter and the connecting DC systems is developed in order to study the impact of non-ideal switches, filters, controls and the interactions with the other HVDC converters. Figure 8 shows the *200MW* test DC/DC converter connecting a *±44kV* DC line to a large *1500MW*, *±250kV* HVDC system. The low voltage *±44kV*, *200km* DC line terminates with an AC/DC VSC converter connecting to a *50kV* AC grid which could represent a local load or a wind farm. The use of DC transformer between HVDC and DC feeders provides following advantages: 1) It lowers DC voltage thus reducing costs for *±44kV* VSC converter and line, 2) It enables DC voltage regulation and thus eliminates an AC transformer on *50kV* grid, and 3) It prevents fault propagation between the main *±250kV* DC line and the local *±44kV* DC line, which is crucial for the operation of such system. The VSC converter assumes a standard 2-level topology with PWM firing control and modulation ratio of *21* [12], and all parameters are in the Appendix.

B. Control strategy

The VSC controller regulates local DC voltage V_{dc} using control signal d component M_d, and the AC voltage V_{ac} using q component M_q.

The DC/DC converter includes an inner DC current feedback PI controller and an outer DC power controller (tap system power). It has been concluded in pervious sections (Figure 5a) that in step down operation I_1 remains constant under V_1 faults. Therefore in step down mode, the inner current controller regulates the "exit current", I_1, to avoid conflict between normal operation and operation under faults. Similarly, in step up operation the inner controller regulates "exit current" I_2. The current reference is made dependent on the terminal voltage (E_1 and E_2) in order to reduce converter power under faults, which is a longer-term fault management strategy (stage 3 converter response), as it is shown in Figure 9.

C. Influence of filters

It is likely that some filtering will be used on DC terminals of this DC/DC converter. A simple shunt capacitor and the conventional shunt filters (C-type, …) have been tested and they did not impact the above converter properties under the fault conditions. Because of the variable frequency operation, a series inductor in addition to shunt capacitor may be effective in improving quality of DC currents equally at low or high voltage terminals, as shown by L_f and C_f in Figure 8. A series inductor will improve the turn off time by reducing the current derivative, and therefore L_{2u} can be reduced, however there is possibility of resonance with shunt capacitors which can cause lingering oscillation under fault conditions.

D. Simulation of DC faults

Figure 10 shows responses for worst case E_2 fault (E_2: *500kV->0kV*). The voltage V_2 (at the converter terminals), in the top graph, reduces at slower rate than E_2, and has a positive value in the instant when the next high-voltage switch is fired. Therefore a filter inductor improves turn off time and clearly the design of L_{2u} and filters should be coordinated.

In Figure 10 we observe that the DC transformer continuously operates through the E_2 fault without internal overvoltage on V_c. It inherently reduces current on low-voltage side as predicted. The current on faulted terminals I_2 shows increase to *5p.u*, in only few pulses. By observing the control input f_s, it is concluded that the controller detects E_2 voltage reduction and reduces the frequency within *10-20ms*. Since operating frequency is reduced, the average fault current in thyristors is reduced and soon the firing gets interrupted altogether to isolate the fault. The *±44kV* VSC converter sees the fault on *±250kV* lines as a gradual load rejection. As it is seen in the lower graph, the VSC converter maintains DC voltage with an overvoltage of *15%* and does not experience any overcurrents.

VII. Conclusions

This paper studies the principles of isolating DC faults using high-power resonant DC/DC converters. It is proven that the resonant DC/DC converter posses inherent stabilising properties that prevent overcurrents and overvoltages in case of terminal faults. The faults on low voltage terminals are particularly well tolerated and only a *10-20%* margin in operating frequency is required to provide satisfactory operation through most severe faults. The faults on high-voltage side are more challenging, but they crucially depend on the suitable size of the step-up inductor on high-voltage side. The high-voltage inductor should be comparable in size to the low voltage inductor to achieve immunity from worst case faults on high voltage terminals. The research demonstrates that the converter is seen as high-impedance circuit on the terminals opposite from faults, for both: low voltage and high voltage faults. While traditional protection strategy reacts to fault currents (detect and open circuit), the present design prevents fault current levels altogether. The converter also well tolerates the unsymmetrical faults.

The detailed PSCAD simulations on a ±44/±250kV test converter in a small DC network, show that there is no fault propagation through DC transformer. A VSC converter on the opposite end of *200km ±44kV* DC feeder very well coordinates fault responses with the DC transformer.

VIII. Appendix Tests system

Table A.1 DC/DC converter parameters

Parameter	*With L_{2u} and L_{2d}*	*Single L_2*
f_s [Hz]	*700*	*330*
V_1/V_2 [kV/kV]	*88/500*	*88/500*
I_{1av} [kA]	*2.27*	*2.27*
I_{2av} [kA]	*0.4*	*0.4*
dI_2/dt [A/μs] (max)	*29*	*8.5*
Vcp [kV] (peak)	*651*	*635*
Efficiency [%]	*98.8*	*98.6*
C_r [μF]	***6.6***	***13***
L_1 [mH]	***28***	***67***
L_2 [mH]	***L_{2u}=14, L_{2d}=4***	***14***
α_{2u} [deg]	*140*	*155*
α_{2d} [deg]	*110*	*124*
C_{f1} [μF]	*150*	*300*
L_{f1} [mH]	*4*	*8*

C_{f2} [μF]	50	100
L_{f2} [mH]	10	20
R_g [Ω]	6000	6000

TABLE A.2 SWITCH DATA IN THE PSCAD MODEL (SILICON POWER)

	T1-T4 (C784)	T5-T8 (C604)
Forward/reverse voltage [kV]	150x4.5=700	150x4.5=700
Average on state current [kA]	1.65	0.4
On resistance [mΩ]	150x0.37=55	150x2.1=220
Off resistance [MΩ]	150x0.03=4.5	150x0.062=9.3
Voltage drop [V]	150x1.1=165	150x0.82=128
Extinction time [μs]	400	400

TABLE A.3 VSC CONVERTER

AC voltage	50kV
DC voltage	88kV
PWM Modulation ratio	21
DC capacitance	200μF
AC inductor	9mH

Table A.4 DC line parameters

	44kV line	500kV line
Resistance [Ω]	1	3
Inductance [H]	0.08	0.4
Capacitance [μF]	6	30

IX. ACKNOWLEDGEMENTS

The Authors are thankful for the financial support from the Royal Academy UK, and National Research Council Canada.

X. REFERENCES

[1] Bahram, M.; at all "Integration of small taps into (existing) HVDC links" *IEEE Transactions on Power Delivery*, Volume 10, Issue 3, July 1995, Page(s):1699 - 1706

[2] Sverre Gilje, "Valhall re-development project, Power from shore" Cigré SC B4 Colloquium, Bergen, June 2009,

[3] D.Jovcic "Off Shore Wind Farm with a Series Multiterminal CSI HVDC" *Electric Power Systems Research, Elsevier, Vol 78, issue 4, 2008, pp 747-755*.

[4] Lianxiang Tang; Boon-Teck Ooi; "Protection of VSC Multiterminal HVDC against DC faults" Proceedings of Power electronics specialists conference, June 2002, Volume 2, Page(s):719 – 724.

[5] Baran, M.E.; Mahajan, N.R.; "Overcurrent Protection on Voltage-Source-Converter-Based Multiterminal DC Distribution Systems" *IEEE Transactions on Power Delivery*, Volume 22, Issue 1, Jan. 2007 Page(s):406 - 412

[6] Nakao, H. at all"DC current interruption in HVDC SF_6 gas MRTB by means of self-excited oscillation superimposition" *IEEE Trans. on Power Delivery*, Volume 16, Issue 4, Oct. 2001 Page(s):687 - 693

[7] Meyer, C.; Kowal, M.; De Doncker, R.W., "Circuit breaker concepts for future high-power DC-applications" *Industry Applications Conference*, 2005.Volume 2, 2-6 Oct. 2005 Page(s):860 - 866

[8] McEwan, P.M.; Tennakoon, S.B. "A two-stage DC thyristor circuit breaker" *IEEE Transactions on Power Electronics* Volume 12, Issue 4, July 1997 Page(s):597 - 607

[9] N.Mohan, TM.Undeland, WP.Robbins, "Power Electronics Converters, Applications and Design," *John Wiley & Sons, 2001*

[10] R.J.King, T.A.Stuart "Inherent Overload Protection for series resonant converter" *IEEE Transactions on Aerospace and Electronic Systems"* Vol AES 19 (6), November 1983, pp 820-830.

[11] D.Jovcic, "Bidirectional high power DC transformer" *IEEE Transactions on Power Delivery*, Vol. 24, issue 4, October 2009, pp 2276-2283.

[12] Jovcic, D.; Lamont, L.A.; Xu, L.; "VSC Transmission model for analytical studies" IEEE PES meeting, Toronto, June 2003, Vol. 3.

XI. FIGURES

List of Figures:

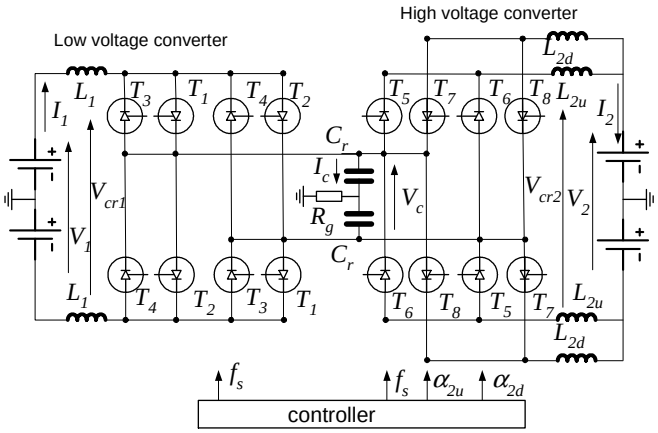

Figure 1. High-Power Bidirectional DC-DC converter (*V2>V1*).

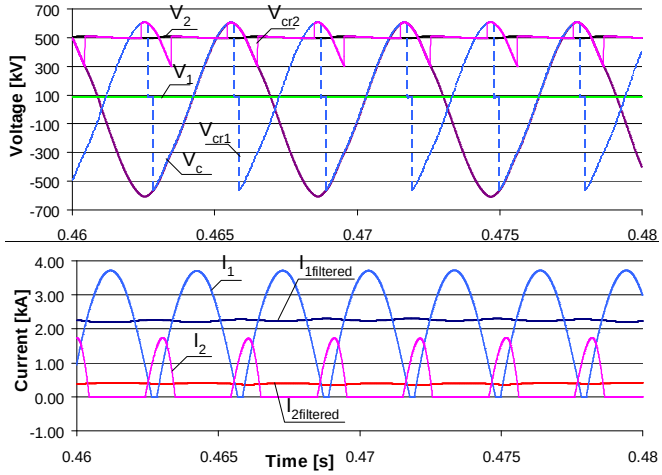

Figure 2. Test system in normal operation. Parameters are given in the Appendix.

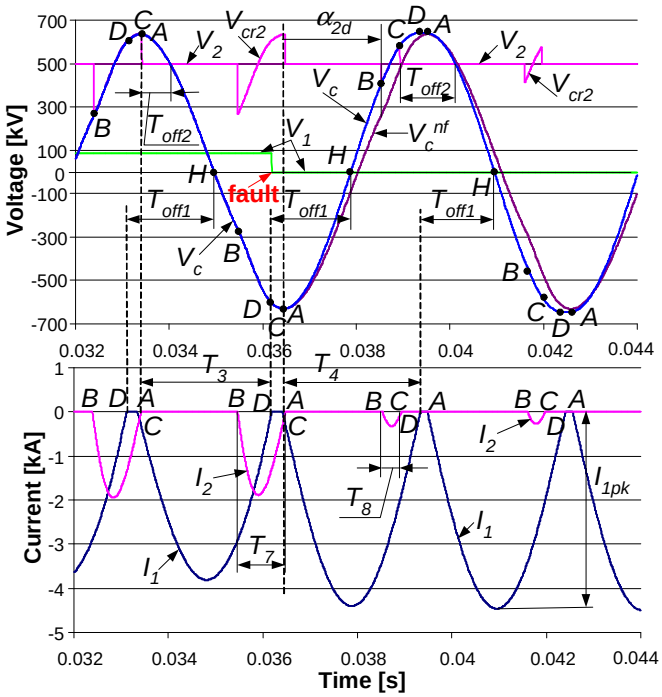

Figure 3 Transient response for a zero-impedance fault on V_1 in step down mode (V_1:*88kV->0kV at 0.036s*, V_2*=500kV*). Top graph: voltages, lower graph: currents.

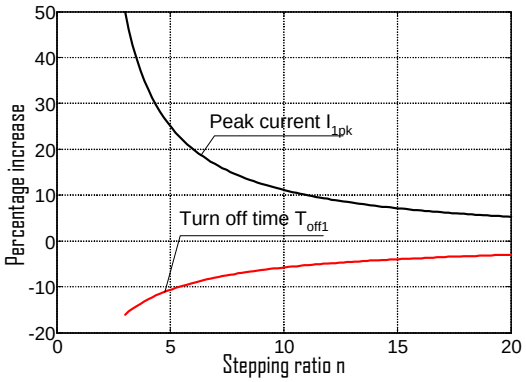

Figure 4. Increase in peak current and turn off time for a zero-impedance fault on V_1.

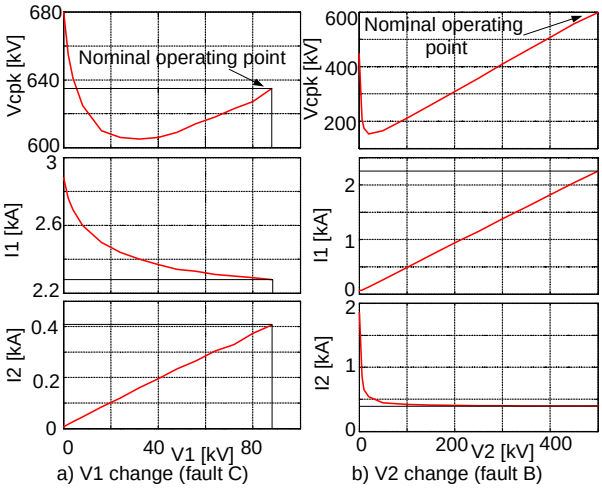

Figure 5. Steady-state converter variables for terminal voltage reduction.

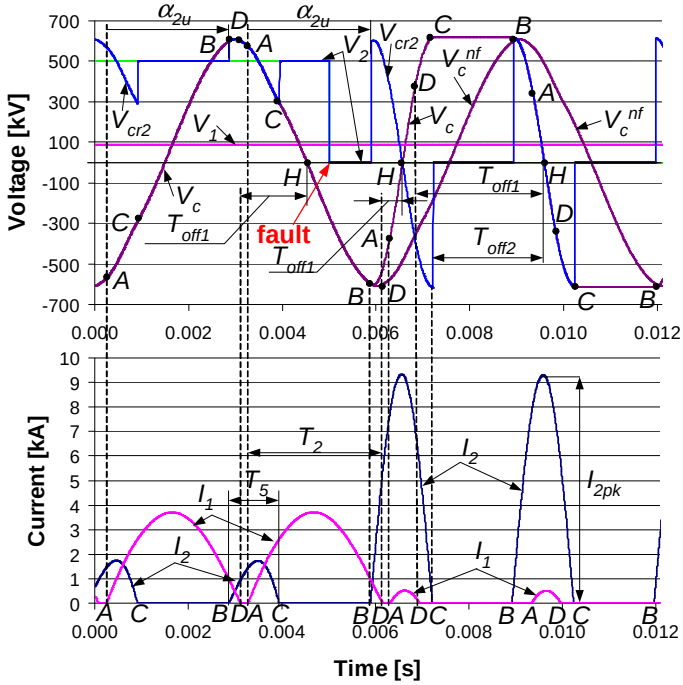

Figure 6. Transient responses for a zero-impedance fault on V_2 in step up mode (V_2*:500kV->0kV at 0.05s*, V_1*=88kV*). Top graph: voltages, lower graph: currents.

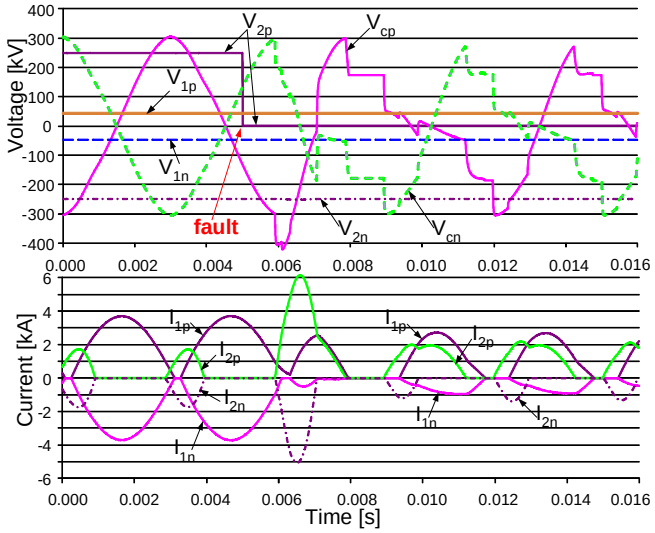

Figure 7. Transient responses for a zero-impedance fault on positive pole V_{2p} in step up mode (V_{2p}*: +250kV->0kV at 0.05s*, V_{2n}*=-250kV*, V_1*=±44kV*). Top graph: voltages, lower graph: currents.

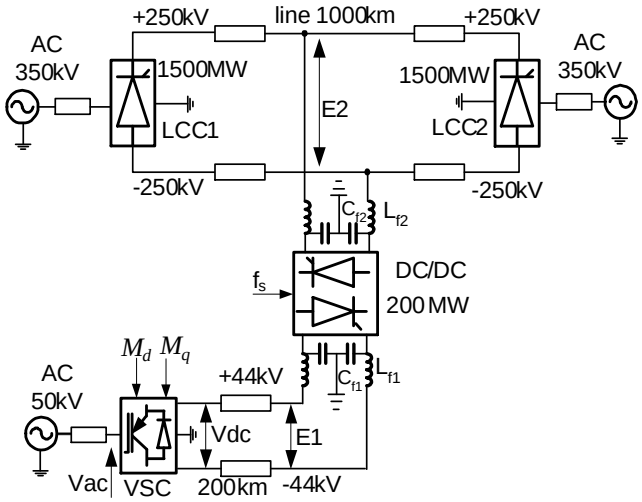

Figure 8. Schematic of tests system with interfacing HVDC converters.

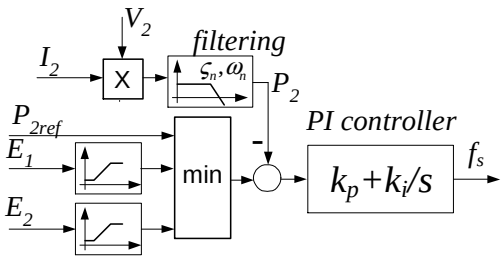

Figure 9. Schematic of DC/DC converter controller.

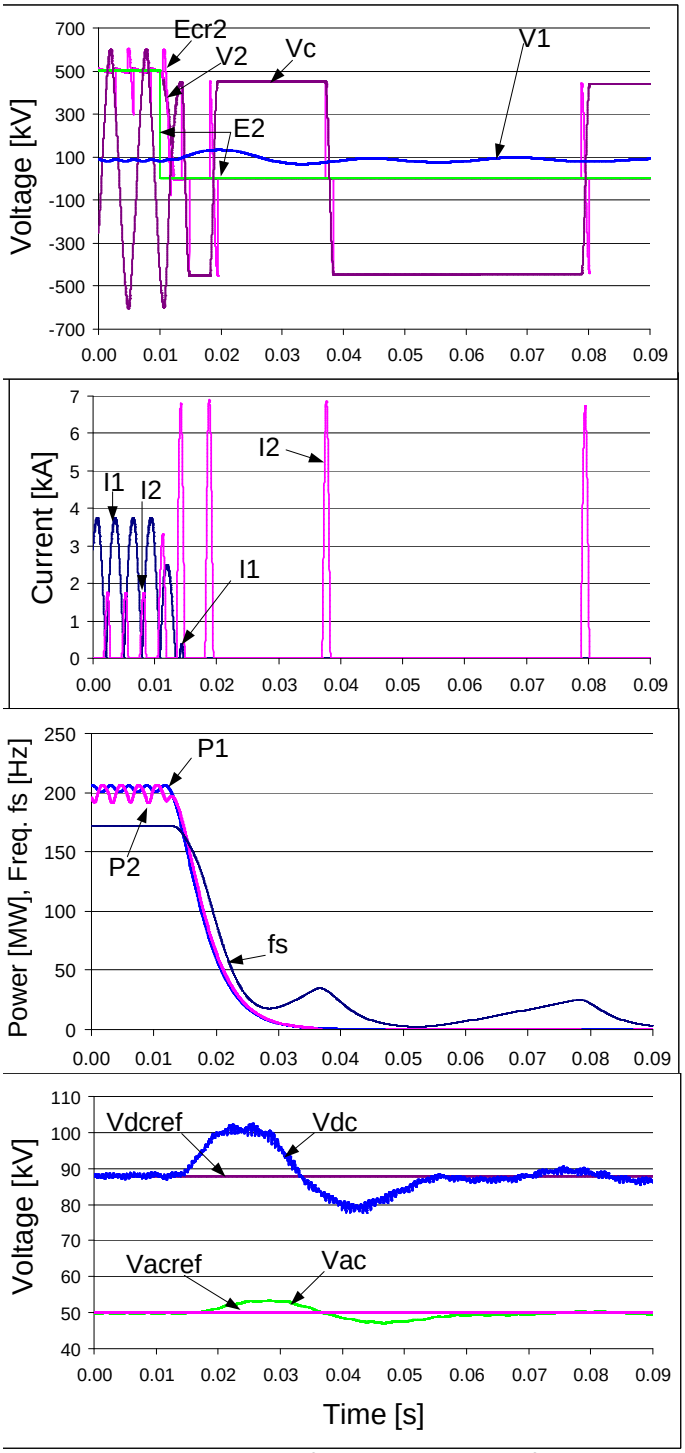

Figure 10. System responses for a low-impedance fault on *500kV* line.